WHAT IS CLAIMED IS:

1. A device for calibrating signals, comprising:

at least two signal circuits configured to generate signals; and

evaluation-drive circuitry configured to evaluate the signals generated by the signal circuits and, dependent thereon, drive at least one of the signal circuits such that a time reference of the signals generated by the signal circuits relative to one another is set corresponding to at least one prescribed value.

2. The device according to claim 1, wherein the evaluation-drive circuitry further comprises at least one comparator that is allocated to the at least two signal circuits and that is configured to compare the signal generated by the at least two signal circuits to one another.

3. The device according to claim 2, wherein the evaluation-drive circuitry further comprises a logic circuit configured to evaluate an output signal of the at least one comparator.

4. The device according to claim 1, wherein the evaluation-drive circuitry further comprises at least one programmable delay loop, and a programmable delay loop is allocated to at least one signal circuit in order to set a delay of the signal circuit.

5. The device according to claim 4, wherein the evaluation-drive circuitry further comprises at least one register and a register in which a delay value can be stored is allocated to at least one programmable delay loop.

6. The device according to claim 5, wherein the at least one register is connected to a logic circuit configured to evaluate an output signal of the at least one comparator via a register bus.

7. The device according to claim 1, wherein the evaluation-drive circuitry further comprises at least one multiplexer to which output signals of comparators are supplied.

8. The device according to claim 7, wherein the multiplexer is controlled by a logic circuit configured to evaluate an output signal of the at least one comparator.

9. The device according to claim 1, further comprising:

a signal generator configured to generate a reference signal with which the signals generated by the signal circuits can be calibrated.

10. The device according to claim 9, wherein the reference signal that is generated by the signal generator is supplied to at least one comparator.

11. The device according to claim 1, wherein the signal circuits are drivers.

12. A semiconductor chip comprising the device according to claim 1.

13. An ASIC comprising the device according to claim 1 that is configured for testing dynamic memory modules.

14. A component comprising the device according to claim 1 for performing a self-test on the component.

15. A method for calibrating signals, comprising:

providing at least two signal circuits for generating signals;

generating signals by the at least two signal circuits;

evaluating the signals generated by the signal circuits; and

driving at least one of the at least two signal circuits such that a time reference of the signals generated by the signal circuits relative to one another is set corresponding to at least one prescribed value.

16. The method according to claim 15, further comprising:

comparing the signals generated by the at least two signal circuits to one another for the evaluation and producing a comparison result.

17. The method according to claim 16, further comprising:

programming at least one of the signal circuits dependent on the comparison result such that the signal it generates is delayed according to the prescribed value.

18. The method according to claim 17, further comprising:

providing a logic circuit comprising an algorithm; and

executing, by the algorithm, the evaluating and programming utilizing the prescribed value.

19. The method according to claim 18, further comprising:

sequentially evaluating, by the logic circuit, a plurality of comparison results.

20. The method according to claim 19, further comprising:

driving, by the logic circuit, for the sequential evaluation of a plurality of comparison results, a multiplexer at whose inputs the comparison results are adjacent.

21. The method according to claim 17, wherein the programming comprises:

driving, by the logic circuit, at least one of at least two registers via a register bus; and

storing a delay value in the at least one register, the at least two registers being respectively allocated to the signal circuits.

22. A method according to claim 21, further comprising:

reading the delay value stored in a register by a programmable delay loop that in turn programs a signal circuit according to the delay value that is read.